



# MimoKit RF Daughterboard

## REFERENCE MANUAL

Version 1.0 – February 15th 2008

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## Revision History

<b>Revision</b>	<b>Date</b>	<b>Author</b>	<b>Comment</b>
1.0	15-Feb-2008	Thierry Durand - Comsis	Document creation

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# 1. About this manual

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## Scope of the Document

The MimoKit hardware system is based on a main PCI board carrying FPGAs, and an optional add-on radio front-end. This document provides the complete functional description of the RF daughterboard. The motherboard is documented separately.

This document includes an architecture overview, a technical description of the major functional blocks and an interface definition. The connector pin-out to the motherboard is covered in detail.

## Intended audience

This document was written for design managers, system developers, ASIC design engineers who are interested in evaluating MIMO technology and performing system prototyping.

Prior knowledge of electronics and RF systems is essential. Working knowledge of the Altera Quartus II environment is necessary to build a design and program the board.

## Using this manual

This document covers the following sections:

- Section 1: this section
- Section 2: generic operation requirements, board handling information and intended use
- Section 3: high level board information, including block diagram
- Section 4: detailed on-board resource information, block by block

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## 2. Introduction

### System Requirements

The RF daughterboard does not have specific system requirements as long as it is used in conjunction with the MimoKit motherboard.

It is recommended to always connect antennas or equivalent 50  $\Omega$  loads on the antenna connectors when the RF daughterboard is powered.

### Purpose of the Board

The RF daughterboard provides the physical radio connectivity to a MimoKit application. It features three identical complete radio stages. Each independent stage is made of a dual-band Baseband to RF transceiver, a Power Amplifier, an antenna switch, and a few filtering and adaptation elements. In order to support true MIMO operation, the three transceivers share the same local oscillator.

The Baseband side of the transceiver is controlled by the mixed-mode circuitry of the MimoKit motherboard (IQ-codecs).

The RF side of the daughterboard consists of three 50  $\Omega$  SMA connectors. Three adapted antennas can be connected to support MIMO configurations up to 3 receive (Rx) by 3 transmit (Tx).

The RF daughterboard embeds both the Radio and its own local power supply. The power supply operation is controlled by the motherboard.

The assembled MimoKit system (motherboard + RF daughterboard) can be used to implement advanced wireless communication systems such as IEEE802.11n access points or terminal stations.

### Handling Precautions

The MimoKit board contains components which are sensitive to electro-static discharge. The board can be permanently damaged if handled without following proper anti-static precautions.



Please do use anti-static precautions when handling the board.

The mating connector between the motherboard and the daughterboard is designed for a limited number of assembly/disassembly cycles. It is recommended not to disassemble the boards unless absolutely necessary. If the daughterboard has to be extracted and re-inserted, care must be taken not to misalign or force the connector.



Parts of the board carry high-frequency signals, possibly at significant power levels. In order to avoid unwanted interference, it is not recommended to alter the topology of the board, or to remove or replace components. As the PCB relies on microstrip techniques, the tracks should not be altered.

During a development phase it may be beneficial to replace the antennas by a wired coax connection. In this case, it is very important to follow these two rules:



- The coax wire must be a 50  $\Omega$  type. Failing to do so will result in part of the RF power being reflected back to the power amp, possibly destroying it.



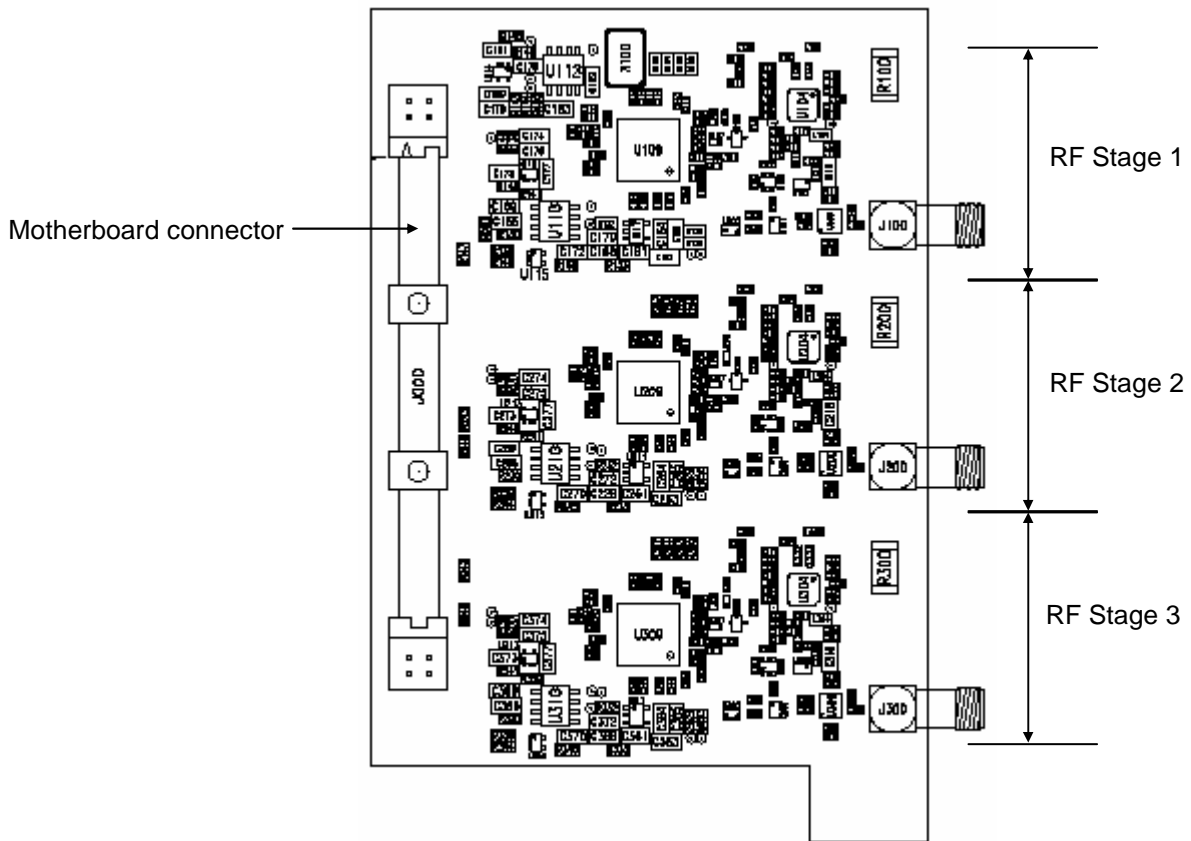
- An attenuator of -20 to -40 dB must be inserted in series with the coax wire. Failing to do so may result in the destruction of the receiving LNA.



### 3. RF Board Architecture

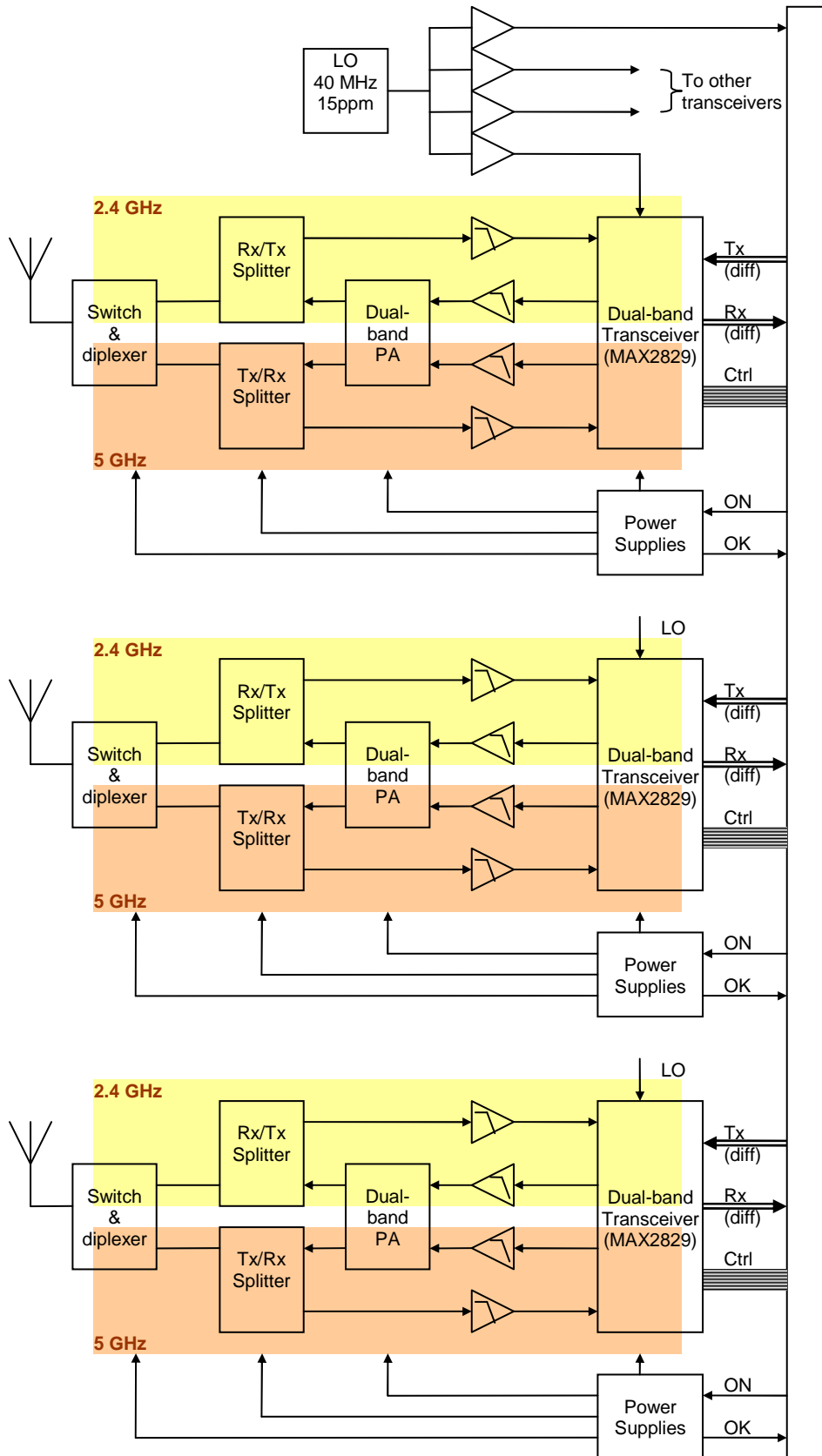
#### A Bird's Eye View of the RF Daughterboard

Illustration 1: Component placement overview



# Block Diagram

Illustration 2: Block diagram of the RF daughterboard



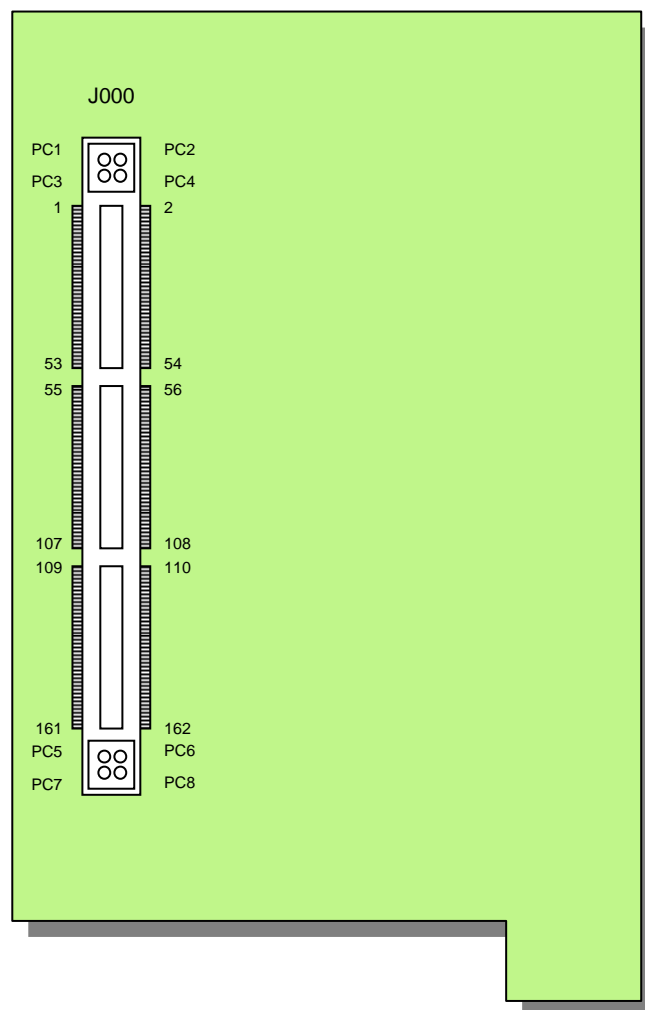
## 4. Board Resources

This section details the hardware resources available on the RF daughterboard, and how they are connected to the motherboard.

### Motherboard Connector

The motherboard connector is an essential resource which will be referred to throughout this document. Illustration 3 gives the connector orientation.

*Illustration 3: Motherboard connector orientation*



The pin assignment of the connector is given in Table 1. The description of the signals is covered in the following sections.

Table 1: Pinout of the motherboard connector

<b>J000 Terminal</b>	<b>Function</b>
PC1	5 V power supply from motherboard
PC2	12 V power supply from motherboard
PC3	Supply ground
PC4	Supply ground
1	Signal ground
2	Signal ground
3	TXBBI+ of transceiver A (U109, pin 16). Positive part of In-phase Tx.
4	TXBBQ+ of transceiver A (U109, pin 18). Positive part of Quadrature Tx.
5	TXBBI- of transceiver A (U109, pin 17). Negative part of In-phase Tx.
6	TXBBQ- of transceiver A (U109, pin 19). Negative part of Quadrature Tx.
7	Signal ground
8	Signal ground
9	RXBBI+ of transceiver A (U109, pin 46). Positive part of In-phase Rx.
10	RXBBQ+ of transceiver A (U109, pin 44). Positive part of Quadrature Rx.
11	RXBBI- of transceiver A (U109, pin 45). Negative part of In-phase Rx.
12	RXBBQ- of transceiver A (U109, pin 43). Negative part of Quadrature Rx.
13	Signal ground
14	Signal ground
15	Shutdown signal of transceiver A (U109, pin 39)
16	Signal B1 of transceiver A (U109, pin 48)
17	SPI chip select of transceiver A (U109, pin 28)
18	Signal B2 of transceiver A (U109, pin 50)
19	Signal ground
20	Signal ground
21	SPI clock of transceiver A (U109, pin 27)
22	Signal B3 of transceiver A (U109, pin 53)
23	SPI data in of transceiver A (U109, pin 26)
24	Signal B4 of transceiver A (U109, pin 54)
25	Signal ground
26	Signal ground
27	Signal ground
28	Signal ground
29	Tx enable of transceiver A (U109, pin 13)
30	Signal B5 of transceiver A (U109, pin 56)
31	Rx enable of transceiver A (U109, pin 41)
32	Signal B6 of transceiver A (U109, pin 1)

<b>J000 Terminal</b>	<b>Function</b>
33	Signal ground
34	Signal ground
35	High-pass filter control of transceiver A (U109, pin 42)
36	Signal B7 of transceiver A (U109, pin 3)
37	PLL lock status of transceiver A (U109, pin 37)
38	Grounded through 1 k $\Omega$
39	Signal ground
40	Signal ground
41	RF switch control for antenna A (U100, pin 3)
42	Power good status of local supply A
43	RF switch control for antenna A (U100, pin 7)
44	Power enable control of local supply A
45	Signal ground
46	Signal ground
47	PA control for the 5 GHz band, stage A
48	High accuracy 40 MHz output to motherboard
49	PA control for the 2.4 GHz band, stage A
50	RSSI output of transceiver A (U109, pin 40)
51	Signal ground
52	Signal ground
53	Shield (ground)
54	Shield (ground)
55	Signal ground
56	Signal ground
57	TXBBI+ of transceiver B (U209, pin 16). Positive part of In-phase Tx.
58	TXBBQ+ of transceiver B (U209, pin 18). Positive part of Quadrature Tx.
59	TXBBI- of transceiver B (U209, pin 17). Negative part of In-phase Tx.
60	TXBBQ- of transceiver B (U209, pin 19). Negative part of Quadrature Tx.
61	Signal ground
62	Signal ground
63	RXBBI+ of transceiver B (U209, pin 46). Positive part of In-phase Rx.
64	RXBBQ+ of transceiver B (U209, pin 44). Positive part of Quadrature Rx.
65	RXBBI- of transceiver B (U209, pin 45). Negative part of In-phase Rx.
66	RXBBQ- of transceiver B (U209, pin 43). Negative part of Quadrature Rx.
67	Signal ground
68	Signal ground
69	Shutdown signal of transceiver B (U209, pin 39)

<b>J000 Terminal</b>	<b>Function</b>
70	Signal B1 of transceiver B (U209, pin 48)
71	SPI chip select of transceiver B (U209, pin 28)
72	Signal B2 of transceiver B (U209, pin 50)
73	Signal ground
74	Signal ground
75	SPI clock of transceiver B (U209, pin 27)
76	Signal B3 of transceiver B (U209, pin 53)
77	SPI data in of transceiver B (U209, pin 26)
78	Signal B4 of transceiver B (U209, pin 54)
79	Signal ground
80	Signal ground
81	Signal ground
82	Signal ground
83	Tx enable of transceiver B (U209, pin 13)
84	Signal B5 of transceiver B (U209, pin 56)
85	Rx enable of transceiver B (U209, pin 41)
86	Signal B6 of transceiver B (U209, pin 1)
87	Signal ground
88	Signal ground
89	High-pass filter control of transceiver B (U209, pin 42)
90	Signal B7 of transceiver B (U209, pin 3)
91	PLL lock status of transceiver B (U209, pin 37)
92	Grounded through 1 k $\Omega$
93	Signal ground
94	Signal ground
95	RF switch control for antenna B (U200, pin 3)
96	Power good status of local supply B
97	RF switch control for antenna B (U200, pin 7)
98	Power enable control of local supply B
99	Signal ground
100	Signal ground
101	PA control for the 5 GHz band, stage B
102	Grounded through 1 k $\Omega$
103	PA control for the 2.4 GHz band, stage B
104	RSSI output of transceiver B (U209, pin 40)
105	Signal ground
106	Signal ground
107	Shield (ground)
108	Shield (ground)

<b>J000 Terminal</b>	<b>Function</b>
109	Signal ground
110	Signal ground
111	TXBBI+ of transceiver C (U309, pin 16). Positive part of In-phase Tx.
112	TXBBQ+ of transceiver C (U309, pin 18). Positive part of Quadrature Tx.
113	TXBBI- of transceiver C (U309, pin 17). Negative part of In-phase Tx.
114	TXBBQ- of transceiver C (U309, pin 19). Negative part of Quadrature Tx.
115	Signal ground
116	Signal ground
117	RXBBI+ of transceiver C (U309, pin 46). Positive part of In-phase Rx.
118	RXBBQ+ of transceiver C (U309, pin 44). Positive part of Quadrature Rx.
119	RXBBI- of transceiver C (U309, pin 45). Negative part of In-phase Rx.
120	RXBBQ- of transceiver C (U309, pin 43). Negative part of Quadrature Rx.
121	Signal ground
122	Signal ground
123	Shutdown signal of transceiver C (U309, pin 39)
124	Signal B1 of transceiver C (U309, pin 48)
125	SPI chip select of transceiver C (U309, pin 28)
126	Signal B2 of transceiver C (U309, pin 50)
127	Signal ground
128	Signal ground
129	SPI clock of transceiver C (U309, pin 27)
130	Signal B3 of transceiver C (U309, pin 53)
131	SPI data in of transceiver C (U309, pin 26)
132	Signal B4 of transceiver C (U309, pin 54)
133	Signal ground
134	Signal ground
135	Signal ground
136	Signal ground
137	Tx enable of transceiver C (U309, pin 13)
138	Signal B5 of transceiver C (U309, pin 56)
139	Rx enable of transceiver C (U309, pin 41)
140	Signal B6 of transceiver C (U309, pin 1)
141	Signal ground
142	Signal ground
143	High-pass filter control of transceiver C (U309, pin 42)
144	Signal B7 of transceiver C (U309, pin 3)
145	PLL lock status of transceiver C (U309, pin 37)

J000 Terminal	Function
146	Grounded through 1 k $\Omega$
147	Signal ground
148	Signal ground
149	RF switch control for antenna C (U300, pin 3)
150	Power good status of local supply C
151	RF switch control for antenna C (U300, pin 7)
152	Power enable control of local supply C
153	Signal ground
154	Signal ground
155	PA control for the 5 GHz band, stage C
156	Grounded through 1 k $\Omega$
157	PA control for the 2.4 GHz band, stage C
158	RSSI output of transceiver C (U309, pin 40)
159	Signal ground
160	Signal ground
161	Shield (ground)
162	Shield (ground)
PC5	Supply ground
PC6	Supply ground
PC7	5 V power supply from motherboard
PC8	12 V power supply from motherboard

## Power Supplies

Each RF stage has its own local power supply. The local power supply takes its main source from the motherboard connector and derives three voltage types:

- A digital supply for the digital part of the MAX2829 transceiver
- An analog supply for the transceiver's Baseband analog circuitry and for the embedded PLL. This supply has low noise characteristics.
- An analog supply for the high frequency parts, especially the power amplifier. This supply is low noise, and high bandwidth in order to cope with the frequent Rx/Tx turnarounds encountered in time division duplex systems.

Each local supply can be individually turned on or off under the control of the motherboard. When turned on, the local supply returns a power good information back to the motherboard, and lights up two LEDs (one for each analog supply). The LEDs are located on the top side of the board (the side which is visible when the daughterboard and the motherboard are mated), in front of their corresponding RF stage.

The power-related signals of the connector are listed in Table 2.

Table 2: Connector's pin assignment for power-related signals

J000 Terminal	Function
PC1	5 V power supply from motherboard
PC2	12 V power supply from motherboard
PC3	Supply ground
PC4	Supply ground
PC5	Supply ground
PC6	Supply ground
PC7	5 V power supply from motherboard
PC8	12 V power supply from motherboard
42	Power good status of local supply A. A logic 1 means that the radio stage A is powered, and power is good. This signal drives a LED on the motherboard.
44	Power enable control of local supply A. A logic 1 enables the power of the radio stage A.
96	Power good status of local supply B. A logic 1 means that the radio stage B is powered, and power is good. This signal drives a LED on the motherboard.
98	Power enable control of local supply B. A logic 1 enables the power of the radio stage B.
151	Power good status of local supply C. A logic 1 means that the radio stage C is powered, and power is good. This signal drives a LED on the motherboard.
153	Power enable control of local supply C. A logic 1 enables the power of the radio stage C.

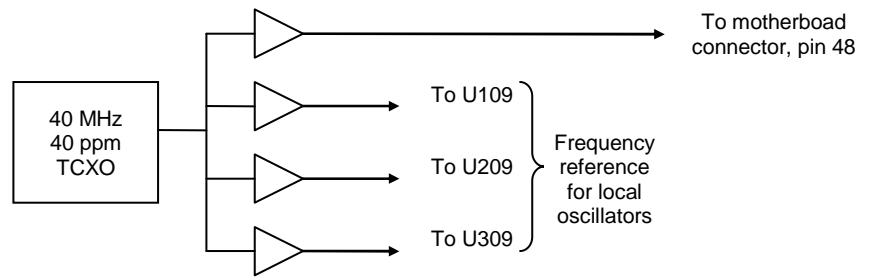
## Reset

The RF daughterboard does not need a separate reset. Most of the components never need a reset. The MAX2829 transceiver is reset by a specific sequence on its functional digital pins. Please refer to the MAX2829 for more information.

## Clocks

The RF daughterboard is basically an analog subsystem which does not need a clock. However the frequency reference of the three transceivers (used to generate the local oscillator via the internal PLL) comes from a high accuracy 40 MHz crystal oscillator which can be used as a clock. This clock signal is buffered on the daughterboard and sent to the motherboard where it can be used as an high accuracy clock by the FPGA1. Please refer to the MimoKit motherboard documentation for more details.

Illustration 4: Clock circuitry of the RF daughterboard. A clock reference is sent back to the motherboard.



## RF Transceivers

The RF daughterboard features three independent Maxim MAX2829 Transceivers. These are dual-band (2.4 GHz and 5 GHz) transceivers integrating many of the analog blocks required to translate the IQ Baseband information to/from the radio spectrum. The MAX2829 has a special operating mode which allows multiple devices to synchronize on the same local oscillator reference. This LO synchronization feature is mandatory in MIMO systems, as each individual MIMO stream must modulate the same carrier frequency. For more information about the operation of the MAX2829, please refer to the Maxim datasheet.

## Baseband Tx Signals

The Baseband Tx signals are directly routed from the motherboard connector to the corresponding inputs of the MAX2829. There are two Tx signals, in-phase (I) and quadrature (Q). Both I and Q are differential, which gives a total of 4 tracks. The individual tracks are carefully routed to minimize differential error and IQ imbalance.

The components driving the analog Tx signals are IQ-DACs located on the motherboard. Since these DACs are current-mode, current-to-voltage conversion resistors are located close to the MAX2829 inputs. All the resistors are matched 49.9  $\Omega$ .

Illustration 5 shows the Baseband Tx circuitry, while Table 3 lists the connector assignment for the Baseband Tx signals.

Illustration 5: Baseband Tx circuitry

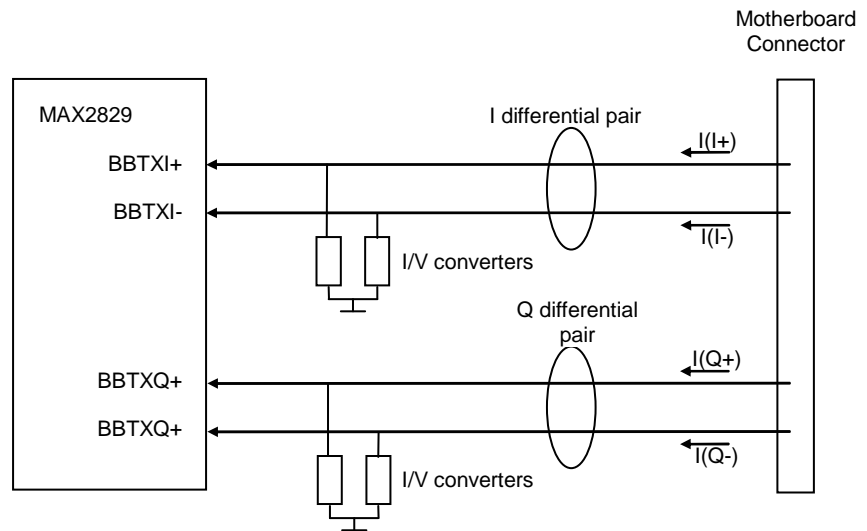


Table 3: Connector's pin assignment for baseband Tx signals

J000 Terminal	Function
3	TXBBI+ of transceiver A (U109, pin 16). Positive part of In-phase Tx.
4	TXBBQ+ of transceiver A (U109, pin 18). Positive part of Quadrature Tx.
5	TXBBI- of transceiver A (U109, pin 17). Negative part of In-phase Tx.
6	TXBBQ- of transceiver A (U109, pin 19). Negative part of Quadrature Tx.
57	TXBBI+ of transceiver B (U209, pin 16). Positive part of In-phase Tx.
58	TXBBQ+ of transceiver B (U209, pin 18). Positive part of Quadrature Tx.
59	TXBBI- of transceiver B (U209, pin 17). Negative part of In-phase Tx.
60	TXBBQ- of transceiver B (U209, pin 19). Negative part of Quadrature Tx.
111	TXBBI+ of transceiver C (U309, pin 16). Positive part of In-phase Tx.
112	TXBBQ+ of transceiver C (U309, pin 18). Positive part of Quadrature Tx.
113	TXBBI- of transceiver C (U309, pin 17). Negative part of In-phase Tx.
114	TXBBQ- of transceiver C (U309, pin 19). Negative part of Quadrature Tx.

## Baseband Rx Signals

The Baseband Rx signals are directly routed from MAX2829 outputs to the corresponding pins of the motherboard connector. There are two Tx signals, in-phase (I) and quadrature (Q). Both I and Q are differential, which gives a total of 4 tracks. The individual tracks are carefully routed to minimize differential error and IQ imbalance.

Note that the MAX2829 outputs are voltage mode. They can be connected to the IQ-ADCs of the motherboard without any additional circuitry.

Table 4: Connector's pin assignment for Baseband Rx signals

J000 Terminal	Function
9	RXBBI+ of transceiver A (U109, pin 46). Positive part of In-phase Rx.
10	RXBBQ+ of transceiver A (U109, pin 44). Positive part of Quadrature Rx.
11	RXBBI- of transceiver A (U109, pin 45). Negative part of In-phase Rx.
12	RXBBQ- of transceiver A (U109, pin 43). Negative part of Quadrature Rx.
63	RXBBI+ of transceiver B (U209, pin 46). Positive part of In-phase Rx.
64	RXBBQ+ of transceiver B (U209, pin 44). Positive part of Quadrature Rx.
65	RXBBI- of transceiver B (U209, pin 45). Negative part of In-phase Rx.
66	RXBBQ- of transceiver B (U209, pin 43). Negative part of Quadrature Rx.
117	RXBBI+ of transceiver C (U309, pin 46). Positive part of In-phase Rx.
118	RXBBQ+ of transceiver C (U309, pin 44). Positive part of Quadrature Rx.
119	RXBBI- of transceiver C (U309, pin 45). Negative part of In-phase Rx.
120	RXBBQ- of transceiver C (U309, pin 43). Negative part of Quadrature Rx.

## RF Signals

The RF side of the MAX2829 is internal to the board and not accessible.

## Control Signals

The MAX2829 uses a number of digital I/O signals to control its internal operation:

- The operational mode and most of the quasi-static features (e.g. the selection of the radio channel) of the MAX2829 are under the control of internal registers. Those registers can be written through a synchronous 3-wire interface (SPI). Each of the three MAX2829 has its SPI ports controllable from the motherboard.
- Some control signals cannot be degraded by the latency of a register write operation. They have dedicated pins with the logic value controlled in real-time from the motherboard. Such signals include the B1..B7 bus used for gain adjustment in the AGC loop, and the direction control signals (TXENA, RXENA).

Table 5 lists the MAX2829 control signals available on the motherboard connector. For more information about the timings and operation of these signals, please refer to the MAX2829 datasheet.

Table 5: Connector's pin assignment for the MAX2829 control signals

<b>J000 Terminal</b>	<b>Function</b>
15	Shutdown signal of transceiver A (U109, pin 39)
16	Signal B1 of transceiver A (U109, pin 48)
17	SPI chip select of transceiver A (U109, pin 28)
18	Signal B2 of transceiver A (U109, pin 50)
21	SPI clock of transceiver A (U109, pin 27)
22	Signal B3 of transceiver A (U109, pin 53)
23	SPI data in of transceiver A (U109, pin 26)
24	Signal B4 of transceiver A (U109, pin 53)
29	Tx enable of transceiver A (U109, pin 13)
30	Signal B5 of transceiver A (U109, pin 56)
31	Rx enable of transceiver A (U109, pin 41)
32	Signal B6 of transceiver A (U109, pin 1)
35	High-pass filter control of transceiver A (U109, pin 42)
36	Signal B7 of transceiver A (U109, pin 3)
37	PLL lock status of transceiver A (U109, pin 37)
69	Shutdown signal of transceiver B (U209, pin 39)
70	Signal B1 of transceiver B (U209, pin 48)
71	SPI chip select of transceiver B (U209, pin 28)
72	Signal B2 of transceiver B (U209, pin 50)
75	SPI clock of transceiver B (U209, pin 27)
76	Signal B3 of transceiver B (U209, pin 53)
77	SPI data in of transceiver B (U209, pin 26)
78	Signal B4 of transceiver B (U209, pin 53)
83	Tx enable of transceiver B (U209, pin 13)
84	Signal B5 of transceiver B (U209, pin 56)
85	Rx enable of transceiver B (U209, pin 41)
86	Signal B6 of transceiver B (U209, pin 1)
89	High-pass filter control of transceiver B (U209, pin 42)
90	Signal B7 of transceiver B (U209, pin 3)
91	PLL lock status of transceiver B (U209, pin 37)
123	Shutdown signal of transceiver C (U309, pin 39)
124	Signal B1 of transceiver C (U309, pin 48)
125	SPI chip select of transceiver C (U309, pin 28)
126	Signal B2 of transceiver C (U309, pin 50)
129	SPI clock of transceiver C (U309, pin 27)
130	Signal B3 of transceiver C (U309, pin 53)
131	SPI data in of transceiver C (U309, pin 26)
132	Signal B4 of transceiver C (U309, pin 53)

J000 Terminal	Function
137	Tx enable of transceiver C (U309, pin 13)
138	Signal B5 of transceiver C (U309, pin 56)
139	Rx enable of transceiver C (U309, pin 41)
140	Signal B6 of transceiver C (U309, pin 1)
143	High-pass filter control of transceiver C (U309, pin 42)
144	Signal B7 of transceiver C (U309, pin 3)
145	PLL lock status of transceiver C (U309, pin 37)

## RSSI Signals

Each MAX2829 provides an analog RSSI (received signal strength information) which is forwarded to the motherboard. The main purpose of this information is to inform the system about the presence of a radio signal in the current channel, and possibly to help in the automatic gain control mechanism.

The RSSI signals are single-ended. They are routed to the motherboard connector as listed in Table 6.

Table 6: Connector's pin assignment for RSSI signals

J000 Terminal	Function
50	RSSI output of transceiver A (U109, pin 40)
104	RSSI output of transceiver B (U209, pin 40)
158	RSSI output of transceiver C (U309, pin 40)

For more information on the AC and DC characteristics of the RSSI signals, please refer to the MAX2829 datasheet.

## Power Amplifiers

Each radio stage has its own independent dual-band Power Amplifier. The selected reference is RF5824 from RF Micro Devices. The maximum output power of this device is 17 dBm, with a gain of 27 dB.

The RF5824 integrates two independent power amplifiers, one for the 2.4 GHz band, and one for the 5 GHz band. Each amplifier has its own enable pin. Although it is technically possible, it is not recommended to enable amplification in both bands simultaneously.

The enable signals of the three RF5824 devices are controlled by the motherboard, as listed in Table 7.

Table 7: Connector's pin assignment for the PA control signals

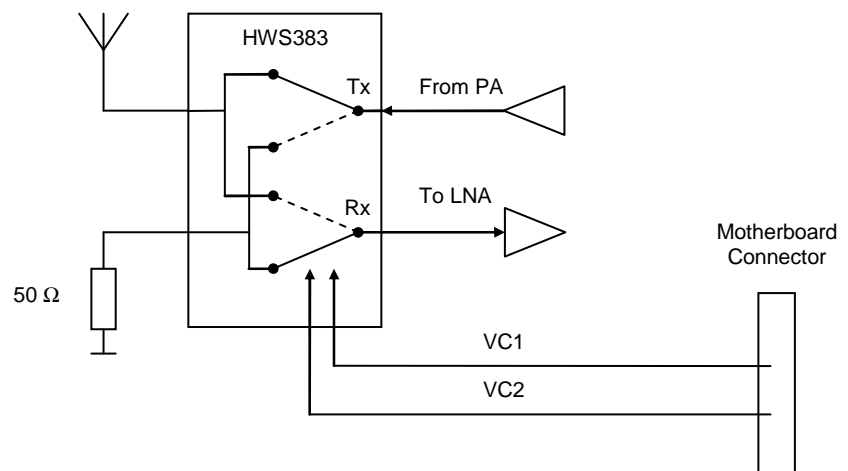
J000 Terminal	Function
47	PA control for the 5 GHz band, stage A 1: enables the PA; 0: disables the PA

J000 Terminal	Function
49	PA control for the 2.4 GHz band, stage A 1: enables the PA; 0: disables the PA
101	PA control for the 5 GHz band, stage B 1: enables the PA; 0: disables the PA
103	PA control for the 2.4 GHz band, stage B 1: enables the PA; 0: disables the PA
155	PA control for the 5 GHz band, stage C 1: enables the PA; 0: disables the PA
157	PA control for the 2.4 GHz band, stage C 1: enables the PA; 0: disables the PA

## Antenna Switches

The TDD duplex is controlled by an RF power switch, the HWS383 from Hexawave. Three instances are used, one per RF stage. The internals of the switch operation are depicted in Illustration 6.

*Illustration 6: Antenna switch topology.*



The logic table for controlling the path is as follows:

*Table 8: Logic table of the antenna switch.*

VC1	VC2	Antenna
0	1	Receives
1	0	Transmits
Other combinations		Not recommended

The switch control signals VC1 and VC2 are routed to the motherboard connector as listed in Table 9.

Table 9: Connector's pin assignment for the antenna switch control signals

<b>J000 Terminal</b>	<b>Function</b>
41	RF switch control for antenna A - U100, pin 3 (VC1)
43	RF switch control for antenna A - U100, pin 7 (VC2)
95	RF switch control for antenna B - U200, pin 3 (VC1)
97	RF switch control for antenna B - U200, pin 7 (VC2)
149	RF switch control for antenna C - U300, pin 3 (VC1)
151	RF switch control for antenna C - U300, pin 7 (VC2)